In the Claims

Claims 1-61 (cancelled).

Claim 62 (currently amended): A semiconductor construction, comprising:

a semiconductive material substrate;

a pair of partially-formed adjacent transistor gates over the semiconductor substrate, the partially-formed transistor gates each having a lowermost layer of conductive material therein, the lowermost layer of conductive material of one of the partially-formed transistor gates being a first segment of conductive material and the lowermost layer of conductive material of the other partially-formed transistor gate being a second segment of conductive material;

a third segment of conductive material extending between the partially-formed adjacent transistor gates and from the first segment of conductive material to the second segment of conductive material; and

~~at least one conductively-doped region~~ one or more conductively-doped diffusion regions within the substrate and directly under the third segment; at least one of said one or more diffusion regions extending from said one of the partially-formed transistor gates to said other of the partially-formed transistor gates.

Claim 63 (currently amended): The construction of claim 62 wherein the at least one of said one or more conductively-doped ~~region~~ diffusion regions ~~includes a pair of regions,~~

~~and wherein at least one of the regions of said pair of regions~~ extends to under at least one of the partially-formed adjacent transistor gates.

Claim 64 (previously presented): The construction of claim 62 wherein the first, second and third segments of conductive material consist of conductively-doped silicon.

Claim 65 (previously presented): The construction of claim 62 further comprising a pad oxide layer beneath the partially-formed transistor gates and beneath the first, second and third segments, and wherein each of the partially-formed transistor gates further comprises;

at least one additional layer of conductive material over the first and second segments of conductive material; and

an insulative layer over the at least one additional layer of conductive material.

Claim 66 (previously presented): The construction of claim 65 wherein the at least one additional layer of conductive material comprises a layer of tungsten over a layer of tungsten nitride.

Claim 67 (previously presented): The construction of claim 65 wherein the insulative layer comprises silicon nitride.

Claim 68 (currently amended): A semiconductor construction, comprising:

a semiconductive material substrate;

a conductive ~~later~~ layer over the substrate, the conductive layer having a thin segment between a pair of thicker segments, one of the thicker segments being a first thicker segment and the other being a second thicker segment;

a first gate stack over the first thicker segment and a second gate stack over the second thicker segment, the first and second gate stacks being spaced from one another by a gap extending over the thin segment;

the first and second gate stacks comprising one or more conductive materials over the thicker segments and comprising one or more insulative materials over the one or more conductive materials; and

at least one conductively-doped region within the substrate under the thin segment.

Claim 69 (previously presented): The construction of claim 68 wherein the one or more insulative layers include a layer comprising silicon nitride.

Claim 70 (previously presented): The construction of claim 68 wherein the one or more conductive materials comprise a layer of tungsten over a layer of tungsten nitride.

Claim 71 (previously presented): The construction of claim 68 wherein the thin segment has a thickness of from about 100Å to about 400Å.

Claim 72 (previously presented): The construction of claim 68 further comprising a masking material over the first and second gate stacks, the masking material having an opening extending therethrough to the thin segment.

Claim 73 (previously presented): The construction of claim 68 wherein the at least one conductively-doped region includes at least one region which extends to under at least one of the first and second gate stacks.

Claim 74 (previously presented): The construction of claim 68 wherein the conductive layer consists of conductively-doped silicon.